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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,601	01/22/2002	Leonard Forbes	303.504US3	8301

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EXAMINER	
SANTIAGO, MARICELI	
ART UNIT	**PAPER NUMBER**
2879	

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/054,601	Applicant(s) FORBES ET AL.	
	Examiner Mariceli Santiago	Art Unit 2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9,12-26,28,29 and 31* is/are rejected.

7)☒ Claim(s) *6,10,11,27 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2, 4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

The Amendment, filed on April 30, 2003, has been entered and acknowledged by the Examiner.

Response to Arguments

Applicant's arguments, see Amendment, Pages 10-11, filed May 5, 2003, with respect to the rejection of claim(s) 1, 3, 9, 10-13, 16, 19, 20, 22, 26 and 27 under 35 U.S.C. 102(b) and the rejection of claims 2, 17, 21 and 24 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-5, 9, 12-17, 19-22 and 26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 33, 35, 36, 41, 46 and 47 of U.S. Patent No. 6,232,705 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Application SN 10/054,601	U.S. Patent No. 6,232,705	Reasons for rejection under obviousness double patenting
Claims 1 and 16	Claim 35	Patent '705 claims a method of forming a field emitter device on a substrate, comprising the steps of forming and utilizing a multiple component mask, wherein separate components of the multiple component mask are used to form selected elements of the field emitter device, forming a polysilicon cone (cathode) on the substrate, forming a porous oxide layer (gate insulator layer) on the substrate, wherein the porous oxide layer (gate insulator layer) and the polysilicon cone (cathode) are formed from a single layer of polysilicon, forming a gate layer on the porous oxide layer (gate insulator layer), isolating the polysilicon cone (cathode) from the gate, and forming an anode opposing the polysilicon cone (cathode).
Claims 2 and 17	Claim 35 in view of claim 33	Patent '705 claims a method wherein forming the field emitter device on a substrate include forming the device on a silicon dioxide (SiO_2) substrate. The Examiner notes that one of ordinary skills in the art would consider an obvious matter of design choice the selection of a known material on the basis of its suitability for the intended use as evidenced by claim 33 of Patent '705.
Claim 3	Claim 35	Patent '705 discloses the use of a multiple component mask, furthermore, a first component (i.e., ONO mask assembly) of the mask is used to form the polysilicon cone and the porous oxide layer, and a second component (i.e., first the oxide layer) is used to form the gate layer.
Claim 4	Claim 35	Patent '705 claims a method wherein masking the cathode region includes forming an oxide-nitride-oxide (ONO) mask over the cathode region, forming the porous oxide layer, removing the top oxide from the ONO mask, etching the nitride to reduce the width of the mask, and forming the gate layer on the porous oxide and the mask.
Claim 5	Claim 36	Patent '705 claims a method wherein forming and utilizing a multiple component mask includes forming an oxide layer over the cathode region, forming a first nitride layer over the oxide layer in order to form a structure which reflects the final pattern of the gate layer, forming a second nitride layer over the first nitride layer and

		the single polysilicon layer, etching the second nitride layer, leaving the second nitride layer only on the sidewalls of the structure, and forming the porous oxide layer, removing the first and second nitride layers, and forming the gate layer on the porous oxide and the oxide layer.
Claims 9 and 19	Claim 35 in view of claim 41	Patent '705 claims a method wherein forming a gate layer on the porous oxide layer (gate insulator layer) include forming a refractory metal gate layer. The Examiner notes that one of ordinary skills in the art would consider an obvious matter of design choice the selection of a known material on the basis of its suitability for the intended use as evidenced by claim 41 of Patent '705.
Claim 12	Claim 46	Patent '705 claims a field emitter device on a substrate, comprising a cathode formed in a cathode region of the substrate, a gate insulator formed in an insulator region of the substrate, a gate formed on the gate insulator, and an anode opposing the cathode the method of forming a field emitter device on a substrate, comprising the steps of forming and utilizing a multiple component mask, wherein separate components of the multiple component mask are used to form selected elements of the field emitter device, forming a polysilicon cone on the substrate, forming a porous oxide layer on the substrate, wherein the porous oxide layer and the polysilicon cone are formed from a single layer of polysilicon, forming a gate layer on the porous oxide layer, isolating the polysilicon cone from the gate, and forming an anode opposing the polysilicon cone.
Claim 13	Claim 46	Patent '705 discloses the use of a multiple component mask, furthermore, a first component (i.e., ONO mask assembly) of the mask is used to form the polysilicon cone and the porous oxide layer, and a second component (i.e., first the oxide layer) is used to form the gate layer.
Claim 14	Claim 46	Patent '705 claims a field emitter wherein masking the cathode region includes forming an oxide-nitride-oxide (ONO) mask over the cathode region, forming the porous oxide layer, removing the top oxide from the ONO mask, etching the nitride to reduce the width of the mask, and forming the gate layer on the porous oxide and the mask.

Claim 15	Claim 47	Patent '705 claims a field emitter wherein forming and utilizing a multiple component mask includes forming an oxide layer over the cathode region, forming a first nitride layer over the oxide layer in order to form a structure which reflects the final pattern of the gate layer, forming a second nitride layer over the first nitride layer and the single polysilicon layer, etching the second nitride layer, leaving the second nitride layer only on the sidewalls of the structure, and forming the porous oxide layer, removing the first and second nitride layers, and forming the gate layer on the porous oxide and the oxide layer.
Claims 26 and 20	Claim 35 in view of claim 34	Claim 26 is rejected for the same reasons stated in the rejection of claim 1 above. Furthermore, while Patent '705 claims a polysilicon cone (cathode), mere duplication of the essential working parts of a device involves only routine skill in the art. Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form multiple polysilicon cones (multiple cathodes) and anodes, since mere duplication of essential parts of the invention is considered within the skill of the art.
Claim 21	Claim 35 in view of claim 34	Patent '705 claims a method wherein forming the field emitter array on a substrate include forming the array on a silicon dioxide (SiO_2) substrate. The Examiner notes that one of ordinary skills in the art would consider an obvious matter of design choice the selection of a known material on the basis of its suitability for the intended use as evidenced by claim 34 of Patent '705.
Claim 22	Claim 35 in view of claim 34	Patent '705 claims a method wherein forming the gate insulator layer include forming a porous oxide layer.

Claims 7, 8, 18 and 28 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 35 of U.S. Patent No. 6,232,705 B1 in view of Lee (US 5,401,676).

Patent '705 discloses the claimed invention except for the limitation of forming a metal silicide on the polysilicon cone (cathode), the metal silicide made by depositing molybdenum (Mo) on the polysilicon cone (cathode). However, in the same field of endeavor, Lee '676

discloses a method for forming a field emitter device wherein forming a polysilicon cone (37) includes forming a metal silicide (40) on the polysilicon cone, the metal silicide made by depositing molybdenum (Mo) on the polysilicon cone. The metal silicide efficiently strengths the emission characteristic of the emitter, and an emitter is made which can block the permeation of the metal component to the insulating layer (Column 4, lines 18-28). Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate the metal silicide made by depositing molybdenum (Mo) on the polysilicon cone (cathode) in order to efficiently strengthen the emission characteristic of the emitter, and provide an emitter which can block the permeation of the metal component to the insulating layer.

Claims 23-25, 29 and 31 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 33, 35 and 41 of U.S. Patent No. 6,232,705 B1 in view of Zimlich et al. (US 5,910,791).

Regarding claims 23, 25 and 29, Patent '705 claims a method of forming a field emitter device on a substrate, comprising the steps of forming and utilizing a multiple component mask, wherein separate components of the multiple component mask are used to form selected elements of the field emitter device, forming a polysilicon cone on the substrate, forming a porous oxide layer on the substrate, wherein the porous oxide layer and the polysilicon cone are formed from a single layer of polysilicon, forming a gate layer on the porous oxide layer, isolating the polysilicon cone from the gate, and forming an anode opposing the polysilicon cone.

Furthermore, while Patent '705 claims a polysilicon cone, mere duplication of the essential working parts of a device involves only routine skill in the art. Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form

multiple polysilicon cones and anodes, since mere duplication of essential parts of the invention is considered within the skill of the art.

Patent '705 is silent in regards to the limitation of coupling a row decoder and a column decoder to the field emitter array, and coupling a processor to the row and column decoders. However, in the same field of endeavor, Zimlich discloses a field emitter device comprising a row decoder and a column decoder coupled to the field emitter array, and further coupling a processor to the row and column decoders in order to operate the device, since it is well known in the art to provide such elements for general driving of the display. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate a row decoder and a column decoder coupled to the field emitter array, and further coupling a processor to the row and column decoders in order to operate the device, since it is well known in the art to provide such elements for general driving of the display.

Regarding claim 24, Patent '705 claims a method wherein forming the field emitter device on a substrate includes forming the device on a silicon dioxide (SiO_2) substrate. The Examiner notes that one of ordinary skills in the art would consider an obvious matter of design choice the selection of a known material on the basis of its suitability for the intended use as evidenced by claim 33 of Patent '705.

Regarding claim 31, Patent '705 claims a method wherein forming a gate layer on the porous oxide layer includes forming a refractory metal gate layer. The Examiner notes that one of ordinary skills in the art would consider an obvious matter of design choice the selection of a known material on the basis of its suitability for the intended use as evidenced by claim 41 of Patent '705.

Allowabl Subject Matter

Claims 6, 10, 11, 27 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mariceli Santiago whose telephone number is (703) 305-1083. The examiner can normally be reached on Monday-Friday from 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (703) 305-4794. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382. Additionally, the following fax phone numbers can be used during the prosecution of this application (703) 872-9318 (for response before a Final Action) and (703) 872-9319 (for response after a Final Action).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MSTg. 7/8/03
Mariceli Santiago
Patent Examiner
Art Unit 2879

Kenneth J. Ramsey
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